ISSN: 2394-7659
IMPACT FACTOR- 2.187

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International Journal of Engineering Researches and Management Studies

A NOVEL HIGH SPEED MAC-16X16 VEDIC MULTIPLIER USING RIPPLE CARRY ADDER ON FPGA

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ABSTRACT

Vedic mathematics is one of the earliest Indian system of mathematics that was rediscovered in the early 20th century This paper proposes the design of high speed MAC-Vedic Multiplier, with the techniques of Vedic Mathematics that have been modified to get better performance using Ripple Carry adders. A high speed processor depends very much on the multiplier as it is one of the solution hardware blocks in most digital signal processing systems in addition to in general processors. Vedic Mathematics has a unique technique of calculations based on sixteen Sutras. we presents design and implementation of high speed MAC-16x16 bit Vedic multiplier architecture which is fairly different from the Conventional method of multiplication like add and shift. Further, the Verilog HDL coding of Urdhva Triyakbhyam Sutra for 16x16 bits multiplication and ripple carry adder is simulated and implemented on XilinxISE9.2i.

KEYWORD:- *RIPPLE-CARRY (RC) ADDER, VEDIC-MULTIPLIER (VM), URDHAVA-TRIYAKBHYAM SUTRA, CARRY SELECT ADDER, VERILOG HDL, MULTIPLIER-ACCUMULATOR(MAC).*

INTRODUCTION

Multiplication is an primary function in arithmetic operations based on this operations, like,Multiply and Accumulate (MAC),[5] and inner product are among some of the frequently used Computation, Intensive Arithmetic and Functions,(CIAF) at present implemented in many Digital Signal Processing(DSP), application like the convolution, Fast Fourier Transform,(FFT) [3], filtering and in microprocessors in its arithmetic and logic unit [1]. Since multiplication dominates the implementation time of a large amount DSP algorithms, so there is a need of high speed multiplier at present multiplication time is silent the dominant factor in determining the instruction cycle moment in time of a DSP chip. The require for high speed processing has been increasing as a result of getting higher computer and signal processing applications.

Advanced throughput arithmetic operations are important to complete the desired performance in many instantaneous signal and image processing applications. The main arithmetic operations in such applications are multiplication and the development of speedy multiplier circuit has been a subject of interest over decades. Dropping the time delay and power consumption are very necessary requirements for many applications. This work presents dissimilar multiplier, architectures.

In this Article a simple 16-bit digital multiplier is proposed which is based on Urdhva Triyakbhyam (Vertically & Crosswise) Sutra of the Vedic Math's. Two binary numbers (16-bit each) are multiplied with this Sutra. The most important concept of this paper is that the speed of propagation and decrease in delay of the conventional, structural design.

This paper is planned as follows. Section II describes basic line of attack of Vedic multiplication, technique. Section III describes the proposed methodology of MAC-Vedic multiplication technique with Ripple Carry adders. Section IV describes the design and implementation of MAC-Vedic multiplier module by using XilinxISE9.2i. Section V, comprise of Result and conversation in which device utilization summary and computational path delay obtain for the projected Vedic multiplier after synthesis is discussed. Finally Section VI comprises of Conclusion.

VEDIC MULTIPLICATION TECHNIQUE

The utilize of Vedic mathematics is to diminish the typical calculations in conventional mathematics to very simple one. for the reason that the Vedic formulae are claimed to be based on the ordinary principles on which the human mind works. Vedic Mathematics is a line of attack of arithmetic rules that allow more capable speed implementation. It furthermore provides some effective algorithms which can be applied to different branches of engineering such as computing [2].

ISSN: 2394-7659
IMPACT FACTOR- 2.187

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The proposed Vedic multiplier is based on the "Urdhva Triyagbhyam" sutra (algorithm). These Sutras have been conventionally used for the multiplication of two numbers in the decimal number system. In this work, we concern the similar ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a universal multiplication formula applicable to all cases of multiplication. It accurately means Vertically and diagonally. It is new concept which is the production of all partial products can be done with the synchronized addition, of these partial, products. The algorithm can be generalized, for n x n bit number. Because the fractional (partial) products, and their sum are premeditated in parallel and the multiplier is independent of the clock frequency, of the processor. Due to its accepted structure, it can be easily layout in microprocessors and designers can without difficulty circumvent these problems to avoid disastrous device failures. The processing power of multiplier can easily be increased by ever-increasing the input and output data bus widths, since it has a quite a regular structure. Due to its regular structure, it can be without difficulty layout in a silicon chip. The Multiplier based on this sutra has the improvement that as the number of bits increases, gate delay and area increases very gradually as compared to other conventional multipliers[3][4][9].

A. Vedic Multiplier for 2X2 bit Module

The method is describe below for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Fig. 1. Initially the least significant bits,(LSB) are multiplied which gives the least significant bit of the last product (vertical). Then, the LSB, of the multiplicand is multiplied with the next higher bit of the multiplier, and added with, the product of List Significant Bit of multiplier and next higher bit of the multiplicand (crosswise). The sum give next bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits,(MSB) to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

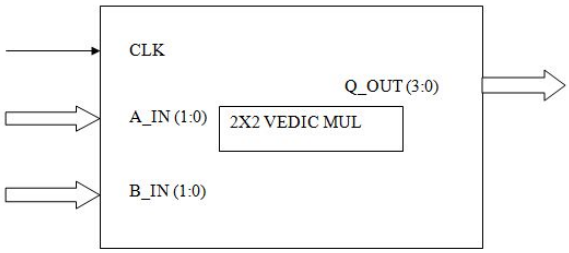

Fig. 1 Block diagram of 2X2 Vedic Multiplier

Consider two inputs, each have 2 bits, say A1A0 and B1B0. Since output, can be of four digits, say Q3Q2Q1Q0. As per fundamental method of multiplication, result is obtained subsequent to getting partial product and performs addition.

A1 A0
* B1 B0
……
A1B0,A0B0
A1B1, A0B1
……..
Q3 Q2 Q1 Q0

In basic Vedic multiplier method [5], Q0 is vertical result, of bit A0, and B0, Q1 is addition of crosswise bit multiplication like A1 & B0 and A0 and B1, and Q2 is another time vertical result of bits A1 and B1, with the carry generated, if any, from the previous addition, during Q1. Q3 output is nothing but carry generated during Q2 result. This module is recognized as 2x2 multiplier block [5, 6, 7,8].

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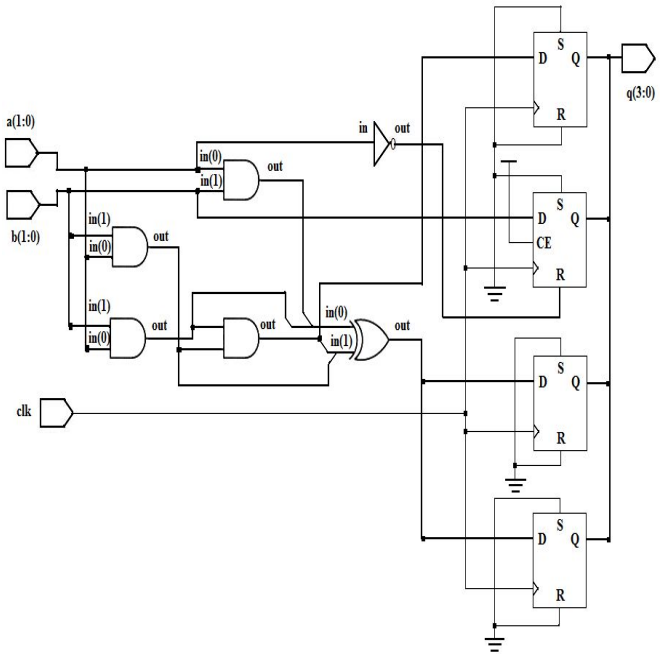

Fig. 2 RTL view of model 2X2 Vedic Multiplier

B. Vedic Multiplier of 4X4 bit Module

For higher no. of bits in input, slight adjustment is required. Separate the no. of bit in the inputs uniformly in two parts.

Assume analyze of 4x4 multiplications, like A3,A2,A1,A0 and B3,B2,B1,B0. Subsequent are the output line for the multiplication result, Q7Q6Q5Q4Q3Q2Q1Q0. Block diagram of 4x4 Vedic Multiplier is given in fig 3,[5].

Let us consider divide A and B into two parts, say A3 A2 & A1 A0 for A and B3B2 & B1B0 for B. Using the basic Vedic multiplication, taking two bit at a time and using 2 bit multiplier block[5,6,7],

A3A2 A1A0
X B3B2 B1B0
……..

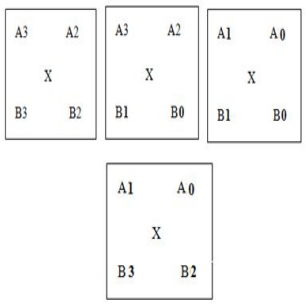

Fig. 3 Algorithm for 4x4 bit Vedic Multiplier

Each block as represent above is 2x2 bits multiplier. Initial 2x2 multiplier inputs are A1 A0 and B1 B0.The end block is 2x2 multiplier by means of inputs A3, A2 and B, B2. The middle one shows two, 2x2 bits multiplier with inputs A3A2 & B1B0 and A1A0 & B3B2. So the last result of multiplication, which is of 8 bit, Q7Q6Q5Q4Q3Q2Q1Q0 [3][5].The 4x 4 bit multiplier is structured with 2X2 bit blocks as shown in figure 4.

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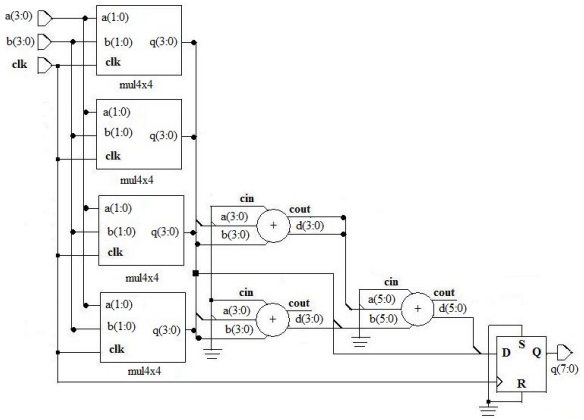

Fig. 4: RTL View model of 4x4 Bit Vedic Multiplier by Model Sim.

C. DESIGN OF 8X8 BITS VEDIC MULTIPLIER

The 8x8 bit multiplier is design by using 4X4 bit blocks as represent in figure 5. In this figure the 8 bit multiplicand A can be disintegrating into pair of 4 bits AH-AL. in the same way multiplicand B can be disintegrating into BH-BL. The 16 bit product can be written as:

P= A * B

= (AH-AL) * (BH-BL)

= AH * BH+AH * BL + AL * BH+ AL * BL

The outputs of 4X4 bit multipliers are added accordingly to obtain the final product. Thus, in the final stage two adders are also required [8],[10],[12].

Now the fundamental building block of 8x8 bits Vedic multiplier is 4x4 bits multiplier which implemented in its basic model. For higher order multiplier implementation like 8x8 bits multiplier, the 4x4 bits, multiplier unit,s has been use as components which is P= A * B

= (AH-AL) * (BH-BL)

= AH * BH+AH * BL + AL * BH+ AL * BL

The outputs of 4X4 bit multipliers are addition as a outcome to obtain the ending product. Thus, in the final stage two adders are also required [5],[11],[12].

The structural modelling of any design shows fastest design [7],[9].

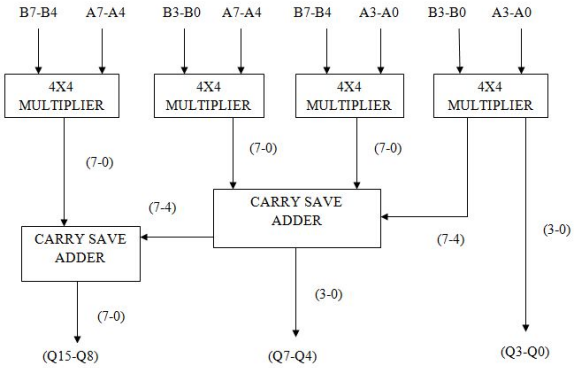

Fig.5 8X8 Bits decomposed Vedic Multiplier

C. IMPLEMENTATION OF 16X16 BITS VEDIC MULTIPLIER

The 16X16 bit multiplier structured using 8X8 bits blocks as shown in Fig. 6. The 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. correspondingly multiplicand B can be decomposed into BH-BL. The outputs of 8X8 bit multipliers are added for that reason to obtain the 32 bits final product. The final stage two adders are also necessary [12]. The structure of 16X16 multiplier is again obtained from the disintegration of 8X8 vedic multiplier,[5].

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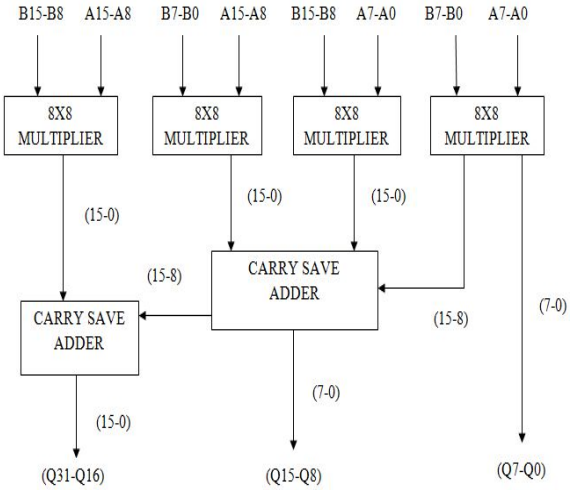

Fig. 6 16x16 Bits decomposed Vedic Multiplier

MAC VEDIC MULTIPLICATION USING RIPPLE CARRY ADDER

The mac-vedic multiplier requires 4 bit, 6 bit, 12 bit, 16 bit , 24 bit adders at every stage of 2X2, 4X4, 8X8 and 16x16 multiplication. The ripple carry adder generally consists of two full adders and a multiplexer. Adding two n-bit numbers by a ripple carry adder is done with two adders (therefore two ripple carry adders) in order to complete the calculation twice, one time with the supposition of the carry individual zero and the other assuming it will be one. After the two results are designed, the correct sum, with the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

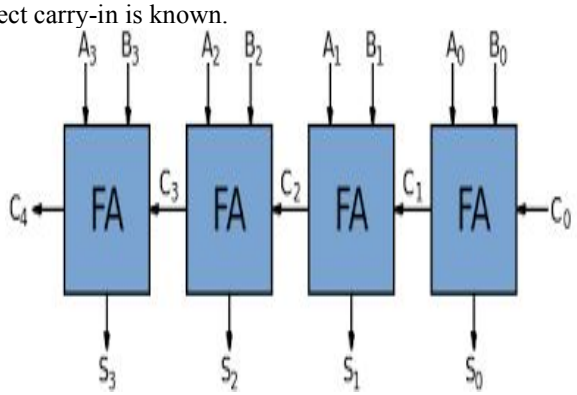

Fig. 3.1 4 bit Ripple Carry Adder

The number of bits in each Ripple carry adder block can be homogeneous, or variable. In the regular case, the most favourable delay occurs for a block size of $\lfloor\sqrt{n}\rfloor$. When changeable, the block size should have a delay, beginning addition inputs A and B to the carry out, identical to that of the multiplexer chain most important into it, so that the carry out is calculated now in time. The $O(\sqrt{n})$delay is derived from homogeneous sizing, where the perfect number of full-adder element per block is equal to the square root of the number of bits individual added, since that will give way an equal number of MUX delays.

In this paper we propose 16X16 mac-vedic multiplier using ripple Carry adders as its one of the basic component of multiplier. This will decrease the area in FPGA and also increase the performance in terms of calculation speed. It will be verified by comparing hardwired unsigned multiplier.

IV Design and Implementation of 16X16 MAC-Vedic multiplier using ripple carry adder

The 16X16 multiplier is implemented and simulation results were tested in XilinxISE8.2i and Model-Sim simulator. Implementation and simulation of its decomposed 8X8, 4X4, 2X2 and ripple carry adder is also done in XilinxISE8.2i.

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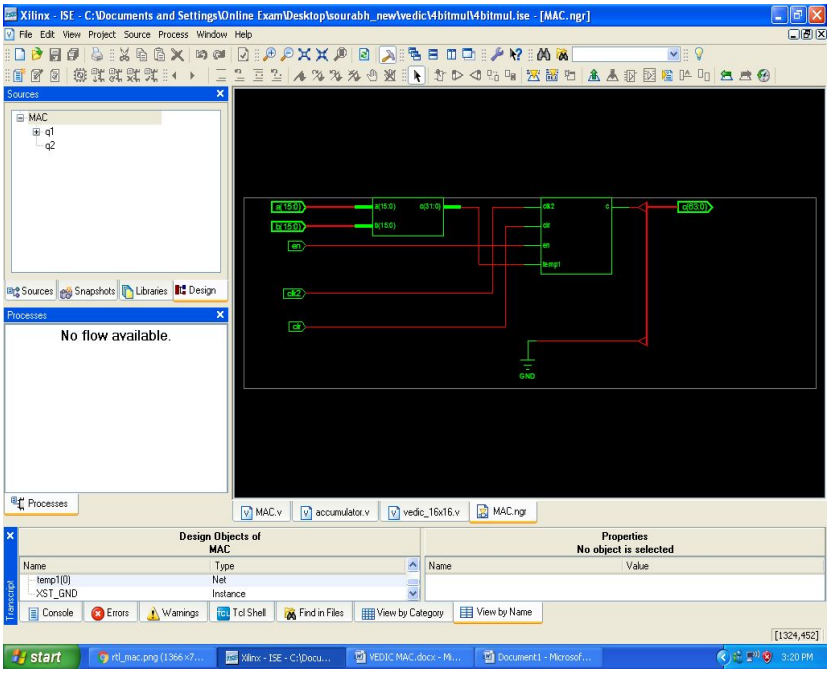

Fig. 16X16 vedic multiplier RTL and components

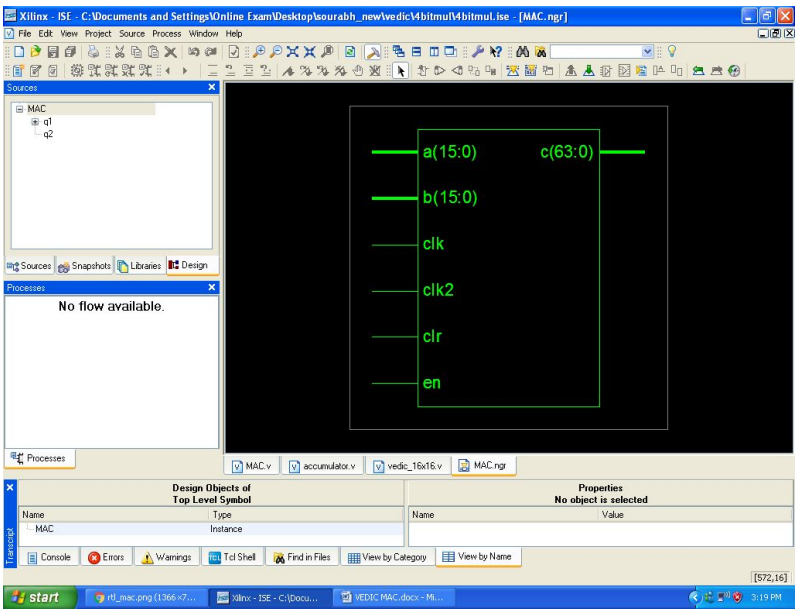

Fig. 16X16 vedic multiplier RTL and components

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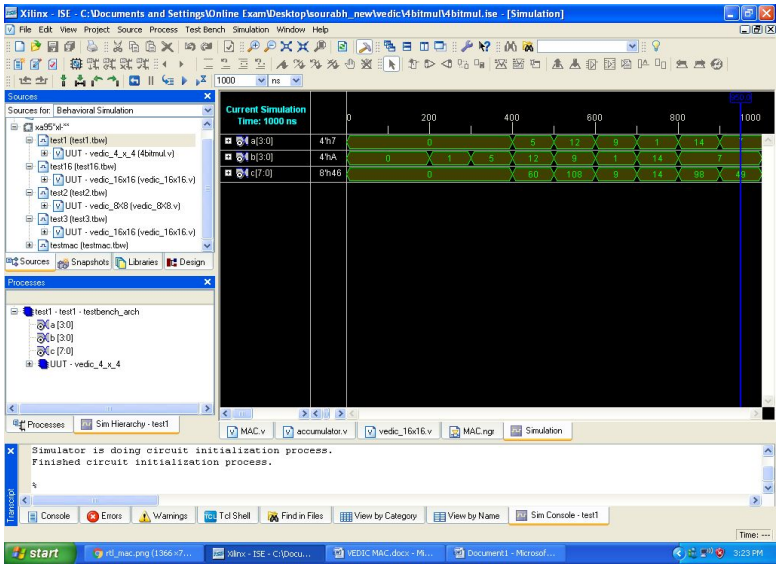

Fig. 16X16 vedic multiplier simulation result

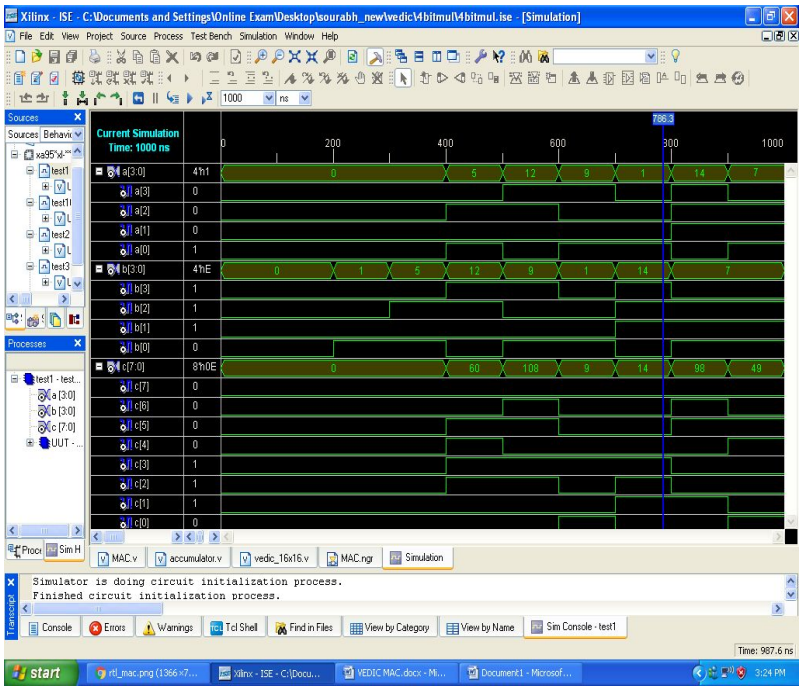

Fig. 16X16 vedic multiplier with MAC simulation result

RESULTS AND DISCUSSION

Simulation of MAC-16X16 vedic multiplier using ripple carry adder shows a great decrease in area and better performance in terms of calculation speed. The area delay product is also decrease but it is greater than a normal udhrava tribhakayam multiplier due to the fact that redundancy in the adder section is increased.

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Type of multiplier	Speed or delay in ns	Area in terms of no of slices	Area delay product
Hardwired multiplier	105ns	1372	144060
Vedic Multiplier	98ns	854	83692
MAC-Vedic multiplier with ripple carry adder	80ns	1130	90400

Table 5.1 Comparison of different multipliers performance in terms of Area and speed

CONCLUSION AND FUTURE WORK

The designs of MAC-16x16 bits Vedic multiplier have been implemented on Spartan XC3S500-5-FG320 device. The calculation delay for 16x16 bits Hardwired multiplier was 110 ns and for 16x16 bits Vedic multiplier was 96 ns. The proposed mac-vedic multiplier with ripple carry adder has a delay of 80 ns only. It is therefore seen that the Vedic multipliers is faster than the conventional multipliers. The algorithms of Vedic mathematics are much more efficient than of conventional mathematics.

Vedic Mathematics, developed about 2500 years ago, gives us a clue of symmetric computation. If all those Technique effectively, implement hardware, it will decrease the computational speed drastically. Therefore, it might be likely to implement a complete ALU using all these methods using Vedic mathematics methods. Vedic mathematics is extended been known but has not been implemented in the DSP and ADSP processors employing large number of multiplications in calculating the a variety of transforms like FFTs and the IFFTs. By using these ancient Indian Vedic mathematics methods world can complete new heights of performance and quality of the cutting edge technology.

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